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Latent Damage and Reliability in Semiconductor Devices

PROJECT PLAN

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1. Summary

This project plan includes a detailed description of our Senior Design Project and how the research will be conducted. We will be discussing our overall goals, previous research in the field, our test procedures, costs, and data analysis.

1.1 Abstract

Latent damage due to an Electrostatic Discharge (ESD) event is a topic of debate within the Semiconductor industry. Our goal, as a team, is to research if latent damage does or does not exist within semiconductor devices after experiencing an ESD event. Our next task is to conclude whether these devices are reliable after proving latent damage exists. Section 4 will explain in detail how the research will be conducted.

1.2 Background

1.2.1 Previous Work Completed

Xuan Zhang, a student who was previously performing this research for Dr. Geiger had a similar goal to ours. She had designed a few Printed Circuit Boards (PCBs) and left those for us to utilize. These boards held two different purposes. One design was going to be used to induce an ESD event on a device. The other design is to be used to monitor multiple devices while accelerating their lifetime. More in-depth details about how we will be using these boards can be found in Section 4.2.1.

1.3 Hypothesis

As a team we expect that if an ESD event occurs on a semiconductor device, then latent damage exists. Furthermore, this latent damage can cause the reliability of these devices to decrease; resulting in the Mean Time to Failure (MTTF) to be substantially shorter than the manufacturing specification.

2. Research

2.1 Summary

A study of previous research was completed to understand the work that has been conducted with respect to semiconductor latent damage. In Section 2.2, a brief summary for each of the most relevant articles has been depicted from our perspective.

2.2 Articles

2.2.1 ESD Induced Latent Defects In CMOS ICs And Reliability Impact

This article was published during the 2004 EOS/ESD Symposium and is highly applicable to our project. The researchers were looking at the ESD effects on bulk 0.6µm p-doped substrate devices: specifically a ring oscillator and a basic differential op-amp. These two devices allowed them to take a look into the different domains of analog and digital circuits.

Their approach was very similar to ours (detailed in Section 4). They started with the device, stressed it, put it in a burn-in oven to accelerate its lifetime, and then tested the device. However, there are some differences in their work compared to ours.

For one thing, they considered and investigated the physical defects in their devices; using two different methods of Failure Analysis (FA) called Emission Microscopy (EMMI) and Optical Beam Induced Resistance Change (OBIRCH). However, we do not have easy-access to labs and the equipment required to make use of these FA techniques. Another difference was the use of multiple voltage levels and impulse counts. Our procedure only requires a single voltage level and impulse count to stress the devices (see Section 4).

Specifically, our team is interested in how an ESD event impacts the lifetime of a Commercial off-the-Shelf (COTS) device; while they were just looking for the physical defects and the impact on electrical performance.

One major finding from their research is noted and might be considered during our testing; their tests showed that analog circuits (the basic op-amps) were damaged through the ground rail of the device. Our team would like to look for this kind of pattern during testing.

2.2.2 Latent Damage due to Multiple ESD Discharges

This article was published during the 2009 EOS/ESD Symposium. The experiments performed were to examine ESD protection diodes after stress events from an ESD gun and also after Transmission Line Pulses (TLP).

A failed device is defined by the researches when a major change in electrical performance is measured: like an open, short, increased leakage current, or reduced breakdown voltage. Our team defines a failed device differently; an inverter that has incorrect logic levels at the input or output (I/O) is a failed device (more details in Section 4.3.3).

Their stress procedure starts with a relatively low voltage level of ten pulses. If the device has not entirely failed, another ten pulses are applied to the sample at a higher voltage. This is continued until the sample has failed. It's important to note the previous voltage level to when the device has failed – this is considered the maximum tolerable stress (voltage) level. We will use a different tactic to determine the maximum voltage level, which is outlined in Section 4.3.

During more sample testing, they also increased the number of pulses being applied to the devices while using the same procedure as above. This showed that the critical stress level is reduced drastically for a higher number of pulses. Essentially, the increase in pulse count will cause the device to fail at a much lower stress level than previously.

When a device failed during any of their tests, it would completely fail with no sign of electrical performance degradation that lead up to the failure. For example, they were able to show that with 80% of the maximum stress level being applied to a diode, the leakage current was at a normal level after 199 pulses. Just after the next pulse (number 200) was applied, the leakage current increased by 5 orders of magnitude which resulted in a complete failure of the device, otherwise called a 'sudden death' failure.

During FA on a sudden death device, using Light Emitting Microscopy (LEM) and OBIRCH, it can be seen that metal alloying is taking place at the edge of the contact area. Metal filaments (spikes) are driven

deeper into the silicon with each additional pulse but this damage cannot be measured electrically until the filaments reach (or short) the p-n junction. As soon as the filament reaches the p-n junction is when the leakage current increases significantly, as mentioned in the previous paragraph.

To conclude, this research has shown that latent damage does exist in common ESD protection diodes during ESD stress pulses. In this specific experiment, electrically measuring the physical damage was not possible until the device had completely failed.

2.2.3 ESD Phenomena in Interconnect Structures

This article was published during the 2003 EOS/ESD Symposium. In summary, physical and latent damage due to ESD events are found in metal interconnects and n-type doped silicon based interconnects. Also, a Transmission Line Pulse (TLP) can cause very similar damage.

According to the article, the author states that when the TLP stress is applied on the device, it leads to discolored spots, open connections, change in line resistance, increase in noise, and reduction of electromigration lifetime. The evaluation on the damage can be measured from the leakage current.

Devices with metal interconnects had small resistance changes after TLP stress was applied. This would not be seen as a functional problem; however, the author mentioned that electromigration lifetime could reduce with a factor of 100 or more in these types of devices.

The n-type doped silicon interconnects had snapback-like behavior during the TLP stress. The snapback phenomenon kept causing junction breakdown between the n-diffusion and the substrate. This type of effect does not stop while applying TLP stress, also leading a resistance change but passing functionality.

Overall, this article includes several sets of test data to show IV characteristics of varying resistance and damage in interconnects. However, it does not have enough information on ESD latent damage and does not mention what kind of semiconductor devices were used in detail. Also, there was not a specific value of TLP voltage listed for their experiments. Thus, the data from this article will not directly influence our hypothesis of whether or not latent damage exists in semiconductor devices after an ESD event.

3. Project Timeline

3.1 Summary

In *Figure 1*, the project highlights and multiple key components have been listed to help manage our time as a team. This schedule will be followed strictly but also adjusted accordingly throughout both semesters of Senior Design. A project timeline is the most important aspect to a project plan and should be taken seriously if success is desired.

3.2 Gantt Chart

	Task Name	Start Date	End Date	% Complete
1				
2				
3	**Fall 2015 Semester**	**08/24/15**	**12/16/15**	
4	Project Assignments	08/25/15	09/01/15	100%
5	Research	09/01/15	10/07/15	100%
6	Website	09/16/15	09/30/15	100%
7	Project Plan V1	09/30/15	10/02/15	100%
8	Order Parts	10/07/15	10/19/15	100%
9	Design Document V1	10/20/15	10/23/15	100%
10	Create & Verify Test System	10/26/15	11/23/15	
11	DUT Functionality System			70%
12	ESD Stressing System			90%
13	DUT Lifetime Acceleration System			30%
14	Test Samples of Devices	11/23/15	11/30/15	0%
15	Prepare Presentation	11/10/15	12/14/15	80%
16	Presentation for Review Panel	12/14/15	12/14/15	
17	**Spring 2016 Semester**	**01/11/16**	**04/29/16**	
18	Multiple Sample Tests	01/11/16	02/08/16	
19	Repeat until Desired Failure Rate			
20	Record Data			
21	Data Analysis	02/08/16	02/22/16	
22	Redesign Test System	02/22/16	02/29/16	
23	Repeat Sample Tests	02/29/16	03/28/16	
24	Data Analysis	03/28/16	04/04/16	
25	Verify Hypothesis	04/04/16	04/11/16	
26	Prepare Presentation	04/11/16	04/27/16	
27	Final Presentation	04/27/16	04/29/16	

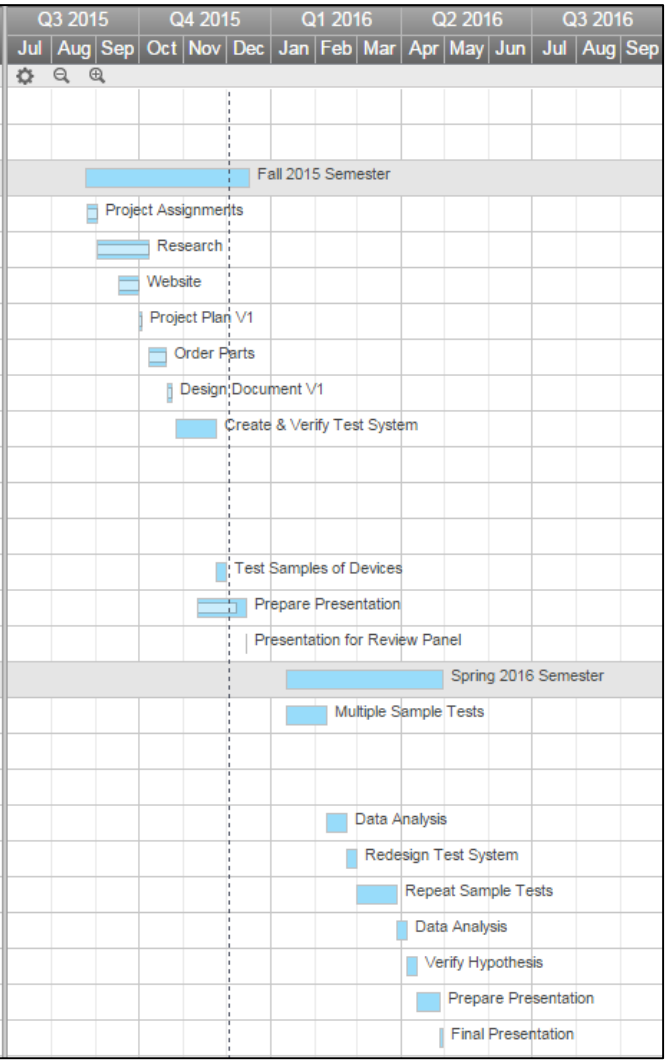

Figure 1: Gantt chart for Project
(Updated on December 3rd, 2015)

4. Test Plan and Procedures

4.1 Summary

Our team has a goal to design and run an experiment to show whether or not latent damage exists in COTS semiconductor devices after an ESD event has occurred. Specifically, our device of interest is a CMOS hex inverter (CD4049UBE) manufactured by Texas Instruments using a bulk-CMOS process.

Latent damage is the type of damage that cannot be measured through the devices electrical characteristics, but a physical defect is present and as a direct result, the device's lifetime is reduced. This kind of phenomenon would mean that our COTS devices can have unforeseen reliability issues, which in turn could mean that present repair procedures (i.e. swapping out boards on a failed system until the functionality returns) for any system undergoing stress could be invalid.

Our primary interest in this project is to electrically stress a large sample of a COTS device by ESD and measure the failure time versus expected lifetime of the devices.

4.2 Test Equipment

4.2.1 ESD Stress PCB & DUT burn-in PCB

The ESD Stress PCB is designed to charge a capacitor via a high-voltage source, and then by flipping a switch, discharge that capacitor to the Device under Test (DUT). This will allow us to simulate an ESD event on a device. Currently, the high-voltage source on the existing board is non-functional due to a previous experiment. Our plan is to use a standalone high-voltage source as an alternative.

The DUT burn-in PCB is used to monitor multiple devices while accelerating their lifetime in a burn-in oven. It has a set of LED arrays which provide output levels of the devices as well as a control switch to vary the input level of the devices.

4.2.2 Burn-in Oven

Under normal operating conditions, the expected lifetime for a COTS device is in the order of decades. To allow completion of this experiment before May of 2016, the lifetime of the COTS devices will need to be accelerated.

It is well known, a device under operation while at a particularly high temperature will experience an accelerated lifetime. To allow the experiment to be completed on the order of months, we will use a burn-in oven to accelerate our parts' remaining lifespan after the ESD stress.

From there, we can test the logical functionality of the devices and record how much longer they last *after* the ESD stress.

However, it should be noted that the existing burn-in boards have outstanding issues. As of right now, when powered, the boards treat an empty socket in the exact same way as a populated socket. Progress has been made toward resolving the PCB issues and will hopefully be resolved soon.

4.3 Testing Procedure

Much of the testing procedure has already been detailed. However, in the interest of completeness and usability of this document, our current plan for testing is detailed here.

4.3.1 ESD Stress

The first part of our experiment will involve taking a sample of 100 COTS devices and subjecting them to a high-voltage ESD event. This procedure will use the PCB described in Section 4.2.1. A capacitor will be charged with a high-voltage source, then discharged into the input gate of a hex inverter. This procedure is ESD stress procedure is repeated for each hex inverter of all 100 COTS devices.

During this type of ESD event, all outputs will be tied low (ground) to put the pMOS transistors in a high-current mode inducing a higher stress condition because of the raise in temperature.

4.3.2 Accelerated Lifetime

Once the devices have been stressed, they will be inserted into a burn-in oven to accelerate their lifetime. As mentioned in Section 4.2.2, this will accelerate the overall lifetime of the devices to much shorter, manageable durations. Keep in mind that the devices will need to be powered-on and kept in the high-current mode during the accelerated lifetime testing. This process is generally called *burn-in*.

4.3.3 Pass & Fail Conditions

Our metric for determining failure of the device during burn-in will be through the logic levels. As each device contains multiple inverters, the status of the LED indicators on the DUT burn-in PCB should be opposite that of the shared input of the testing board. A failure will be considered when any of the inverters on a device have incorrect logic.

Figure 2

Input	Output
0	1
1	0

The truth table of a single inverter is shown in *Figure 2*. If at any time a single inverter has an incorrect logic level, then the DUT has failed. At which point, the device lifetime will be recorded for later analysis.

Given this, it will also be worth noting *how* the device failed. Is the device always giving a high output? Is the device always giving a low output? Or is it giving reverse operation? Which one of these three possible outcomes occurs for failed devices might also be worthwhile to study for our project. If a pattern emerges, it may suggest that the pull-up network (PUN) or pull-down network (PDN) of COTS devices are more vulnerable to ESD events and latent damage. If so, this may have further implications for future studies and preventative measures.

4.4 Data Analysis

Just collecting raw data isn't enough to draw a conclusion. Statistical analysis must be performed to make a conclusion about our results.

4.4.1 Mean Time to Failure (MTTF)

The basis for determining the existence (or non-existence) of latent damage is through the mean lifetime of the parts, or the Mean Time to Failure (MTTF).

As it may be obvious, a higher MTTF in our sample (as compared to a control group) would be counter-intuitive. This would imply that the ESD event actually *helped* our COTS part last longer! What we're expecting, should latent damage exist, is for the sample's MTTF be lower than our control groups'.

4.4.2 Statistical Analysis

However, just having a lower MTTF isn't enough to conclude that our devices actually have latent damage that was caused by the ESD stress.

Because of the nature of semiconductors, we cannot say with 100% certainty that our sample was valid. Due to variance in any manufacturing process, some devices will last an exceptionally long amount of time, while others will fail immediately. We must use statistical testing to generate a high confidence level of our MTTF being lower.

The sample size of 100 is large enough for us to apply the Central Limit Theorem, which will allow us to treat the sample as a Normal Distribution. From there, it's a matter of using procedures from statistics courses.

We'll start with a hypothesis and calculate a P-value based off of it. From that P-value, we can either reject the hypothesis or confirm it. In both cases, our conclusion will be based on the results from the statistical analysis.

4.5 Safety Concerns

Safety during this experiment is definitely of great importance. The dangers to us during experimentation are the high temperatures of the burn-in oven and the high-voltages used to perform the ESD stress.

The current plan is to use a standalone, commercial device to produce the high-voltages. However, it can't be expected that this device will be able to output high amounts of *energy*. Still, the higher voltage needs to be considered and isolated from other conductive sources to prevent arcing.

The burn-in oven also could pose burn hazards, but not any more dangerous than a standard conventional oven. After placing boards in the burn-in oven for a desired amount of time, we will need to use heat-resistant mitts to handle the boards and devices.

4.6 Advantages & Disadvantages

There are, of course, advantages and disadvantages of our experimental approach.

If latent damage is found, it can be found valid only for COTS devices, specifically hex inverters. This can be seen as an advantage or disadvantage.

Another disadvantage of our approach is that we also are not looking at the electrical properties of the devices. While latent damage shouldn't have an impact on the electrical properties of the DUT, there could still be non-latent damage we weren't measuring.

However, this approach does give us advantages. The test structure doesn't need to be designed from scratch. Further, we also have a rather simple procedure for the measurements and data analysis.

5. Bill of Materials

In *Figure 3* you will find our most updated copy of the Bill of Materials. This table includes all of the parts and components we will need to purchase or have already purchased in order to successfully complete our experiment and research. Our total project cost cannot exceed $1,200 – as defined in the proposal.

Bill of Materials						*Updated: December 3rd 2015*
Item	Qty.	Reference	Cost	Part Description	Supplier	Supplier #
1	1	M20	$53.49	Fence Energizer (High-voltage source)	Gallagher	M20
2	1	DEFT-Z	$36.37	Digital Electric Fence Tester	Zareba	DEFT-Z
3	50	10M Resistors	$7.88	RES MF HV .25W 10M OHM 1% AXIAL	Digi-Key	RNV14FAL10M0CT-ND
4	10	DHRB34A101M2BB	-	Murata Ceramic Disc Capacitors 100pF +/-20%	Mouser	81-DHRB34A101M2BB
5	500	CD4049UBE	-	TI Hex Inverters	Digi-Key	296-2055-5-ND
6	2	Custom	-	ESD Stress PCB	-	-
7	10	Custom	-	DUT burn-in PCB	-	-
TOTAL COST			$97.74			

Figure 3: Bill of Materials

6. Risks & Feasibility

6.1 Profitability Risks for Industry

Integrated circuit (IC) manufacturing is very costly. One way to reduce the overall cost is to reduce the amount of internal ESD protection that a circuit has. However, this can lead to severe consequences for the consumer or user after the ICs are implemented in a system. The ESD protection circuitry is costly, but if it is implemented, an increase in product quality and product reliability can be seen. The cost to replace a damaged device can range from few cents (for a simple diode) to hundreds of dollars for a complex IC (Intel CPU).

Our goal is to prove that latent damage exists in COTS semiconductor devices after an ESD event on the system. If latent damage exists; consumers, manufacturers and suppliers will have to consider the overall reliability of each device in an ESD-stressed system. This will most likely require that every device on the stressed system be replaced by a brand new device – which would be costly and undesirable.

6.2 Feasibility of Semiconductor Devices

It is said that the ESD events occur multiple times every single day; however, most of the people do not notice their exposure to electronic devices. For example, you may see that keypads or buttons do not work properly because of an ESD event. These days, most semiconductor devices are treated as static sensitive devices such as MOSFETs because these devices have high impedances. To prevent ESD events, a variety of protection devices are used for electronic devices: anti-static mats, ESD benches, ESD bag, ESD wrist straps, and etc. These lead to overcome and guarantee the long term reliability of the devices.

7. Conclusion

After conducting our research we hope to have either proved or disproved our hypothesis. We will have successfully completed our experiments in a safe manner and will have stayed within our desired budget.

The semiconductor industry may disapprove of our research if we conclude that latent damage does indeed exist. Latent damage existing after an ESD event within a COTS device would decrease the reliability. This decrease in reliability might push the functionality of the device outside of the manufacturers' specifications, which could lead to undesirable profit loss.

There are many opportunities of growth for this type of research on semiconductor devices. We have simply performed a small portion on a specific COTS device and hope to encourage others to do the same.

8. References

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